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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/798,227	02/11/97	KEETH B	660073.587

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EXAMINER	
RANSOM, D	
ART UNIT	**PAPER NUMBER**
2752	7

DATE MAILED: 09/11/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/798,227	Keeth
Examiner	**Group Art Unit**
David Ransom	2752

☒ Responsive to communication(s) filed on *Aug 3, 1998*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-19* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-19* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1 through 6 and 8 through 11 and 13 through 15 rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent number 5,577,236}. Text of this section not found here may be found in a prior office action.

The applicant amends claim 1 with transmitting control data from the memory controller to the memory device for revising the initial output timing in response to the identified phase error to produce a revised output timing. Johnson provides for this with column 5 line 48 through

column 6 line 46. The applicant amends claim 1 with revising the initial output timing at the memory device according to the control data. Johnson provides for this with column 6 lines 8 to 46. The applicant amends claim 11 with a second input coupled to the clock bus to receive echo signals and phase output coupled to the logic circuit. Johnson provides for this with column 9 lines 39 to 51. The applicant amends claim 13 with a memory controller including a master clock generator coupled to the clock bus to generate a master clock signal, a phase comparator having a first input coupled to the master clock generator and a second input and responsive to a phase difference between the first and second inputs to produce an adjust command and a logic circuit. Johnson provides for this with column 5 line 48 through column 6 line 46. The applicant amends claim 13 with an echo signal generator to generate an echo signal responsive to the master clock signal at the clock input. Johnson provides for this with column 6 lines 8 to 46. The applicant amends claim 13 with the delay circuit being responsive to the adjust command on the command bus to produce the control signal at a time corresponding to the adjust command. Johnson provides for this with column 8 lines 1 to 32.

The applicant amends claim 14 with a second input coupled to the echo signal generator and a phase output coupled to the logic circuit. Johnson provides for this with column 8 lines 1 to 32.

5. Claims 16 through 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent number 5,577,236}.

The applicant amends claim 16 with a method of adjusting data timing in a memory system having a memory device and a memory controller. Johnson provides for this with column 5 lines 15 to 33. The applicant amends claim 16 with the method comprising the steps of transmitting the first sets of data, receiving the first set of data, establishing an initial output timing, transmitting a second set of data, receiving the second set of data, comparing the second set of data, transmitting a third set of data and revising the initial output timing. Johnson provides for this with column 5 line 48 through column 6 line 46. The applicant amends claim 16 with transmitting a first set of data to the memory device according to a first clock signal. Johnson provides for this with column 5 line 48 through column 6 line 8. The applicant amends claim 16 with receiving the first set of data at the memory device. Johnson provides for this with column 5 line 48 through column 6 line 8. The applicant amends claim 16 with establishing an initial output timing at the memory device having a default phase relationship with the first clock signals. Johnson provides for this with column 6 lines 8 to 46. The applicant amends claim 16 with transmitting a second set of data from the memory device to the memory controller according to the initial output timing. Johnson provides for this with column 6 lines 8 to 46. The applicant amends claim 16 with receiving the second set of data at the memory controller. Johnson provides for this with column 6 lines 18 to 46. The applicant amends claim 16 with comparing the second set of data to the first clock signal in order to identify a phase error. Johnson provides for this with column 6 lines 8 to 46. The applicant amends claim 16 with transmitting a third set of data from the memory controller to the memory device for revising the initial output timing in

response to the identified phase error. Johnson provides for this with column 6 lines 8 to 46. The applicant amends claim 16 with revising the initial output timing at the memory device according to the third set of data to produce a revised output timing. Johnson provides for this with column 6 lines 8 to 46.

The applicant amends claim 17 with the step of transmitting a second set of data includes transmitting an echo clock signal. Johnson provides for this with column 6 lines 8 to 18.

The applicant amends claim 18 with the step of comparing the second set of data comprises the steps of generating a plurality of phase shifted signals, comparing the echo clock signal, identifying one of the phase shifted signals and generating a third set of data. Johnson provides for this with column 8 lines 1 to 32. The applicant amends claim 18 with generating a plurality of phase shifted signals responsive to the first clock signal. Johnson provides for this with column 8 lines 1 to 32. The applicant amends claim 18 with comparing the echo clock signal to each of the phase shifted signals. Johnson provides for this with column 6 lines 8 to 46. The applicant amends claim 18 with identifying one of the phase shifted signals having a phase within a selected range of phases relative to the echo clock signal. Johnson provides for this with column 8 lines 1 to 32. The applicant amends claim 18 with generating the third set of data according to the identification of the phase shifted signal. Johnson provides for this with column 6 lines 8 to 46.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. {US Patent number 5,577,236} as applied to claim 6 above, and further in view of Smith {US Patent number 5,020,023}. Text of this section not found here may be found in a prior office action.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. {US Patent number 5,577,236} as applied to claim 6 above, and further in view of Smith {US Patent number 5,020,023}. Text of this section not found here may be found in a prior office action.

10. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. {US Patent number 5,577,236} as applied to claim 6 above, and further in view of Smith {US Patent number 5,020,023}.

Johnson discloses the invention substantially as claimed. However, Johnson does not disclose a vernier. Smith teaches the use of a vernier as a source of creating a harmonic frame that last for a predetermined period of time. The applicant amends claim 19 with the step of

revising the initial output timing at the memory device includes the step of adjusting a vernier. Smith provides for this with column 6 line 60 through column 7 line 21.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to us the digitally enhanced vernier signal generator as a source for the clock pulse in the analogous art of time-keeping for the purpose of providing a more accurate clock signal that is useable for digital systems. This signal generator will be accurately reproducible with clock pulses that are a fixed phase from the main pulse cycle. The counter is adjustable for higher processor clock speed by adding more counter line space or a time divider circuit that will clock the computer at slower rates than its source clock. The fixed delay is computable from the original signal in order to create a desired phase after the original signal with flexibility and room for expansion.

Response to Arguments

11. Applicant's arguments filed August 3, 1998 have been fully considered but they are not persuasive.

The applicant argues a method of adjusting data timing and controlling data flow in a memory system by revising the relative phase relationship between clock signals of the memory controller and clock signals of a memory device. The examiner finds this irrelevant because of the comparison of the response by the memory for the system clock with the five phase clock signals will result in the ability to determine if there is a lead or a lag in the clock response time. The

phases are preselected to give the ability of the controller to determine if the memory is operating at faster speeds than expected or slower. The options include faster, much faster, slower, much slower and normal speed. The controller finds which line produces the best return to determine phase expectancy modifications required for the optimum speed of the memory chip. The applicant argues with assume that an initial output timing is established at the memory device. The memory device transmits data to the memory controller data (either read data or an echo clock signal) based on the initial output timing. The memory controller will then identify any phase error of the transmitted signal relative to a clock signal in the memory controller. The examiner finds this irrelevant because the memory device is still synchronized to the system clock. The memory device has two signals that it may create in response to the command. The first response is the data that is normally given to the bus for system processing. The second is a data/ clock signal that may take the form of an automatic toggle or a clock reflection. In either case the leading edge of the pulse indicates the position of the data change. The result of the phase error will result in the comparison at the controller of the reflected signal for expected time delay. The applicant argues based on the identified phase error, the memory controller will transmit some control data that will be used by the memory device to revise the output timing that was initially established. The subsequent transmission of data from the memory device to the memory controller will be based on the revised output timing. The examiner finds this irrelevant because of delay circuits that are used to create a new base reference. This base reference may generate a new place to time the controller for the controllers clock. The applicant argues the Johnson

patent discloses a memory system where the memory controller has a system clock circuit generating a system clock signal that is fed to the memory bank and (an inverted system clock signal) to the command driver. The command driver sends read commands to the memory bank according to the system clock signal. The examiner finds this irrelevant because the memory will normally be responsive to the system clock. Upon surpassing the 33 MHz clock speed, processors became too quick for their remote devices like I/O and memory. Bus mastering and buffering was used to overcome the difficulties of multiple clock pulses on the processor bus per clock pules on the system bus. As processors became faster, they relied on their cache memory and bus master for data handling. RAM on the system bus utilizes the slower clock frequency. The primary item on the system bus to be used is the memory. Rarely will the data bypass the memory to go to the I/O devices. The applicant argues the memory controller of the Johnson patent also has a sampling clock circuit providing multiple sampling clock signals, each having a phase shift relative to the system clock change. A multiplexer selects one of the sampling clock signals to be fed into a delay module, the output of which is fed to a first receiver that synchronizes a latch to accept read data transmitted by the memory bank. The examiner finds this irrelevant because of the need for the ability to translate from one phase to another require a standard of determining the error of the signal. Without this phase error creator, either by generation or by logic or by delay circuit, there will be no practical way to determine if a hit was on time, early or late. The applicant argues the delay module preferably includes an off-chip supplementary delay unit of a fixed value. The delay value can be adjusted only by physically

replacing the off-chip delay unit with one having the desired delay value. The examiner finds this irrelevant because of the desire for adjust-ability will cause the designer to create a source of variation if updating the delay line is to be of importance. If this is not adjustable, this method of testing the delay will be of little purpose outside of the quality control department of the factory. This lack of purpose will result in a redundant device that is consuming resources with little ability, except to act as an indicator for the user when the computer bus is over active and may be acting up.

The applicant argues a section of which sampling clock signal to feed to the delay module is based on information fed to the multiplexer from the data source. The examiner finds this irrelevant because it is a comparison of the data response against the clock responses. The data may be just the data requested, data with clock like pulses included in it, or a logical analysis of data compared to the last data. The important part of the data comparison is checking for changes in the data. The applicant argues the information coming from the data source may be provided by either automatic or manual means. Once the information in the data source is established, the multiplexer cannot select any other sampling clock signal until the information in the data source is either reprogrammed or manually changed. The examiner finds this irrelevant because the calls to memory are request for access to a data. There is no limitation in this invention to one cell versus block data requests. Usually the request to memory are in block format. The applicant argues the Johnson patent does not disclose a structure or operation where the memory controller identifies a phase error. The examiner finds this irrelevant because of a

phase comparator created by the data created by the comparison of the clock reflection to the selected clock phase line. The latched data will tell the memory how to adjust the clock by the comparison of the digital data produced in comparing the two lines. Captured data may be compared with original data to give the computer an idea on the delay involved. The applicant argues the structure disclosed by the Johnson patent is designed such that the memory bank transmits only read data to the memory controller. There are no clock signals transmitted by the memory bank to the memory controller as with embodiments of the present invention. The examiner finds this irrelevant because of the transmission of read data that is already performed on the computer by a memory read command. Read data will be as reliable as a clock pulse as long as it changes state. A series of toggle data will best perform this data test. The applicant argues the selection of the sampling clock signal in the Johnson system cannot be changed without physically changing switches or reprogramming a flash memory. The examiner finds this irrelevant because of sampling clock signals are based on the system clock and subsequently delayed by the delay line. Adjustment to the delay line should provide all the flexibility that this device needs. The applicant argues although the structure disclosed in the Johnson patent does include a delay module, the delay value is fixed and cannot be modified without replacing the off chip delay unit with a desired delay value. The examiner finds this irrelevant because of the desire for adjust-ability will cause the designer to create a source of variation if updating the delay line is to be of importance. If this is not adjustable, this method of testing the delay will be of little purpose outside of the quality control department of the factory. This lack of purpose will result

in a redundant device that is consuming resources with little ability, except to act as an indicator for the user when the computer bus is over active and may be acting up.

The applicant argues claim 1 specifies a method of adjusting data timing in which the output timing at the memory device is initially determined and is then subsequently revised. The output timing at the memory device is revised by first "transmitting an echo clock signal from the memory device to the memory controller according to the initial output timing". After each echo clock signal is received at the memory controller, the memory controller identifies "a phase error of the received echo clock signal relative to the master clock signal" and "transmits control data to the memory device for revising the initial output timing in response to the identified phase error to produce a revised output timing". Thereafter, the memory device revises the initial output timing to transmit a second set of data to the memory controller according to the revised output timing. The examiner finds this irrelevant because of the ability to create a data entry that toggles or otherwise carries clock information. The clock return line may be placed on the bus so as to allow synchronization with data reception. The comparison circuit may create data for use by the controller on delay requirements and bus loading. The applicant argues the system disclosed in the Johnson patent does not include a memory device that transmits an echo clock signal to a memory controller according to an initial output timing. Instead, as claimed above, the Johnson memory device transmits only read data to the memory controller. The examiner finds this irrelevant because of the data being used, as before mentioned to carry timing signals useable as a clock. Routines may be made for testing the data and common data may provide sufficient

variations for such a test. The applicant argues furthermore the Johnson patent does not disclose a memory controller that identifies a phase error between a received echo clock signal relative to a master clock signal. The examiner finds this irrelevant because of the use of the phased signals to provide reference points for comparison with the incoming data signal with clock information. The applicant argues, nor does the Johnson system transmit data to the memory device to revise the initial output timing in response to the identified phase error. The examiner finds this irrelevant because of the data comparison is collected to allow for timing alterations. The entire exercise is to allow for manual if not automatic alterations of the reference voltage.

The applicant argues claim 6 is also not anticipated by the Johnson patent because it specifies that the memory device produces an echo signal in response to a first read command and transmits the echo signal to the memory controller. The examiner finds this irrelevant because of that is the idea of the echo clock in order to find a phase or other delay by the bus to the memory. The applicant argues as explained above, Johnson's memory device transmits only data to the memory controller, it does not transmit a clock or echo signal to the memory controller. The examiner finds this irrelevant because of the timing information that may be carried with data, as stated in a prior paragraph. The applicant argues claim 6 further specifies that the memory controller compares the received echo clock signal to a master clock signal and uses that comparison to select an adjusted time delay. The examiner finds this irrelevant because of the time delays importance in solving the element of delay for maximizing the use of the frequency by allowing for the highest frequency to be used without using multiple clock cycles to perform a

single bus access. The applicant argues the memory device then responds to a second read command by transmitting a second set of data to the memory controller with the adjusted time delay. The examiner finds this irrelevant because of the repetitive nature of this command response action. The cycle may be repeated for different phase differences as Johnson has pointed out. The applicant argues as further explained above, the Johnson system does not include any circuitry for performing these functions. The examiner finds this irrelevant because of the request/ response combination present in the invention. The request is presented with a clock signal and the response returns with the data. The applicant argues claim 10 is directed to a memory controller for a memory system containing memory devices that produce echo signals in response to master clock signals applied to a clock bus from a master clock source in the memory controller. The examiner finds this irrelevant because of the memory controller generating a read command in response to the clock pulse. This read command is received by the memory and acted upon accordingly. The memory responds to the read command with data that indicates the time delay between the first command and the second command. The applicant argues the memory controller includes a phase comparing circuit that produces a phase signal in response to a phase difference between the echo signal and the master clock signal. The claim further specifies that the memory controller includes a logic circuit that produces adjustment data in response to the phase signal and a control data circuit adapted to produce a command signal in response to the adjustment data. The examiner finds this irrelevant because of their ability to build a comparator that latches the data response, compares that response to the expected

response and relays the information to a control device to maintain synchronization of data receipt by the controller and action on the data by the controller.

The applicant argues claim 13 is directed to a memory system including a memory controller and a memory device interconnected by various buses. The examiner finds this irrelevant because of the presence of a clock input separated from a address bus, data bus and control bus. The applicant argues the memory device is specified as having an echo signal generator that generates an echo signal in response to a master clock signal. The examiner finds this irrelevant because of the data response could be used or contain clock response information. The applicant argues the memory device further includes a data latch that transmits data to a data bus responsive to a control signal applied to trigger input of the latch. The examiner finds this irrelevant because this latch is used to capture the data signal for determination of its arrival relative to the selection signal. The applicant argues finally the memory device includes a variable delay circuit that responds to an adjust command on a command bus to produce the control signal at a time corresponding to the adjust command. The examiner finds this irrelevant because of the collection of capture data to determine if the delay of the clock is sufficient for activating the control signals. The applicant argues claim 13 further specifies that the memory controller includes a phase comparator that produces an adjust command responsive to a phase difference between a master clock signal from a master clock generator and an echo signal from the echo signal generator. The examiner finds this irrelevant because of the memory comparator claimed in Johnson involving the latching of the data with respect to one of the 5 phase lines. The applicant

argues the Johnson system does not have a phase comparing circuit which compares the phase difference between a signal transmitted by the memory device and a clock signal of the memory controller. The examiner finds this irrelevant because of the ability to catch a signal with respect to previously generated phase standards to determine if the signal went through. The applicant argues the system shown in figure 3 and described in column 5 line 19 through column 7 line 40 does not include a phase comparing circuit that compares the phase error between a clock signal transmitted from the memory bank to the memory controller or a logic circuit that produces a signal in response to the output of the phase comparing circuit. The examiner finds this irrelevant because of the phase caught by the latch contains data on when the data is received and when it is not. This reception will be from the first arrival on until the pulse is stopped. The applicant argues what is shown and described is a system where the clock signal is selected by providing to a multiplexer predetermined information encoded in a hardware data source. The examiner finds this irrelevant because of the use of only one circuit at a time is the purpose if this multiplexer. If 5 comparison latches were provided, resulting in the requirement for a data line buffer, the response will be quicker but slower. If the data line is not buffered, the parallel taps will drain the data bus of current and the data may loose shape. The multiplexer avoids both problems. The applicant argues none of the clock signals can be modified (i.e. the relative phase relationship of the output of the sampling clock is fixed) nor can the selection of which clock signal to transmit to the delay module be changed unless the predetermined information from the hardware data source is reprogrammed or manually switched. The examiner finds this irrelevant because of the delay

module, which may be altered to allow for more or less delay. Failure to provide this variable delay will result in the failure of the circuit to fulfill its primary purpose. The applicant argues furthermore, additional delay of the selected clock signal is possible only by inserting a fixed, off-chip delay unit with another fixed delay unit having a different delay value. The examiner finds this irrelevant because of the delay module has a supplemental delay module to allow fine tuning of the delay provided in the system.

The applicant argues claim 7, which is dependent on claim 6, adds the limitation of adjusting a vernier to select the adjusted time delay. The examiner finds this irrelevant because of the automatic adjustment of the fractional frame skew for vernier synchronization. The applicant argues after the memory device transmits an echo clock signal to the memory controller, the echo clock signal and the master clock signal are compared to determine their relative phase difference. The examiner finds this irrelevant because of the response created by the memory may be used to represent clock response data for comparison by the system. The applicant argues adjustment of the vernier is made based on the relative phase error determined from the comparison. The examiner finds this irrelevant because of the skew is of a fractional frame type. The controller, if it operating as a bus master, may be using the higher speed processor bus rate as a source for this vernier generator. The applicant argues the smith patent discloses a system using a FIFO buffer and a technique of marking frames of a data stream to remove skew between multiple correlated synchronous data streams. The examiner finds this irrelevant because of the requirement of the buffer or latch to catch the data so that it may be sent to its appropriate destination.

Synchronization to this level requires that the data will be captured at that location, and not further down the line. The applicant argues data is placed into a FIFO register with the frame encoding and then removed from the FIFO buffer when the data is to be consumed. The examiner finds this irrelevant because data when not requested individually will transport in burst in order to minimize address identification. Burst start at one location in memory and increment until they reach the second location. This requires only two addresses to be transmitted instead of the addresses for every cell requested. Address translation can triple the data transfer time in the best case. Usually this is a grossly conservative ratio, as the CAS and RAS strobes usually are maintained for several clock cycles each. The applicant argues if a synchronization fault is detected when the data is unloaded from the FIFO buffer, a re-synchronization procedure is triggered. The examiner finds this irrelevant because this is what the device is looking for so it could re-synchronize the data transfer. The applicant argues the procedure described in the Smith patent entails inhibiting the unloading and loading of the FIFO buffer, purging the FIFO buffer, reloading the data into the FIFO buffer while monitoring for the next frame mark and when the next frame mark is detected, re-enabling normal loading and unloading of the FIFO buffer where unloading starts with the frame marked data. The examiner finds this irrelevant because of the eventual necessity of these events in any attempt of burst mode data transfer. The applicant argues the Smith patent uses the term "vernier synchronization" and "vernier skew compensation" to simply describe the fact that frame synchronization used by the disclosed system may be made by adjusting in increments of fractional frame skew, as compared to whole frame synchronization.

Smith's use of vernier has nothing to do with disclosing or suggesting adjusting a vernier in adjusting a time delay in response to the relative phase relationship between two signals. Smiths reference to vernier simply describes making adjustments in less than whole increments. The examiner finds this irrelevant because of the ability to use a vernier by the controller allows for the utilization of a higher frequency to generate a lower frequency base. This lower frequency base can be transmitted as a clock signal and the higher frequency provides an excellent way to create a delay that is variable and precise. Counters may capture counting information so as to provide a this delay, once a value is reached, the clock fires a phased delay. The 16 bits of counter is based on frame size, something that the phase delay can alter to meet its needs.

The applicant argues claim 12, which is dependent on claims 10 and 11, describes the memory controller as having a signal source that includes a multiple delay-locked loop. As referenced by the examiner, the Jeddeloh reference describes the use of phase locked loops (not a delay locked loop) in the prior art as an ineffective means of resolving problems associated with signal skew in high speed data processing environments. The system disclosed in the Jeddeloh patent is designed to overcome the deficiencies by realigning a skewed clock signal to a second skew clock signal by adding an overall alignment delay equal to the sum of the propagation delays of the skewed clock signal. The examiner finds this irrelevant because of the use of either the inserted delays or the phased locked loops to provide sufficient delay to allow the comparison of data to a phase delay standard. Jeddeloh does not limit himself to just phase detection means with this. A phase locked loop locks a phase difference between two harmonic signals. A delay locked

loop locks a time delay between two harmonic signals. A delay allots a predetermined time of delay between two signals. Therefore the examiner fails to find any benefit worth noting or limitation from using a delay locked loop in place of an inserted delay. The loop is maintained for harmonics purposes, and is therefore necessary for a phased locked loop. If a delay locked loop uses both functions, any reference to both functions should allow its use. The applicant argues the deficiencies of the Johnson patent, as discussed above, are not made up for by the Jeddeloh reference. The Jeddeloh reference mentions the use of phase locked loops. In contrast, applicant claims a delay-locked loop in the signal source in order to produce a plurality of phase-shifted signals. Jeddeloh fails to mention a delay-locked loop at all. The examiner finds this irrelevant because of the skew being created by either inserted delays or the phased locked loop.

Conclusion

12. Any response to this action should be mailed to:
Commissioner of patents and trademarks
Washington, D.C. 20231
or faxed to: (730)308-9051 (for formal communications intended for entry) or (703)308-9051 (for informal or draft communications, please label "PROPOSED" or "DRAFT"); Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA 22209, sixth floor receptionist.

Any inquiry concerning this communication should be directed to David Ransom at telephone number (703) 305-4035. The examiner can normally be reached on Monday through Friday from 9:00 to 5:00. If there is any problem contacting me call Tod Swann at (703)308-7791. The fax number to this office is (703)308-5357.

Any inquiry of a general nature or relating to the status of this applications or proceeding should be directed to the group receptionist whose telephone number is (703)305-3900.

David Ransom
David Ransom

Patent Examiner
Group 2752

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER